160 Gbit/s optical packet switching using a silicon chip

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***Abstract*— We have successfully demonstrated 160 Gbit/s all-optical packet switching based on cross-phase modulation using a silicon chip. Error free performance is achieved for the 4-to-1 switched 160 Gbit/s packet.**

Keywords-Optical packet switching; Cross phase modulation; Silicon nanowire.

I. Introduction

The continuous growth of the Internet demands more and more bandwidth. It's therefore envisioned that optical interconnects at the network node will carry data at bit rates above 100 Gbit/s. To support these demands, high-speed optical packet switching has been proposed as excellent candidate for future networks, due to its high throughput, rich routing functionalities and flexibility [1-2]. Furthermore, optical signal processing using silicon chips has attracted considerable research interest, due to its complementary metal-oxide-semiconductor (CMOS) compatibility, low cost, ultra-compactness, integration potential with electronics, broad working bandwidth and high-speed operation [3-7]. In addtion, optical signal processing functionalities where many bits are processed in a single device has been identified as a potentially energy-efficient solution [8]. All-optical packet switching of ultra-high bit rate OTDM signals is such a functionality. Therefore, silicon chip based all-optical packet switching of >100 Gbit/s data packets is highly desirable, but has not been addressed yet.

In this paper, we experimentally demonstrate all-optical packet switching for 160 Gbit/s Ethernet packets in an 8.6-mm long silicon nanowire based on cross phase modulation (XPM). 1 of 4 packets at the bit rate of 160 Gbit/s is switched by an optical control signal. Error free performance is achieved for the switched packet.

II. Experimental Setup

The key device in the silicon chip based optical packet switching experiment is a dispersion engineered 8.6-mm long silicon waveguide, which includes tapering sections for low loss interfacing with optical fiber. The main waveguide section is ~8 mm long and has a cross-sectional dimension of 240 nm × 450 nm while the tapering sections are ~0.3 mm long each. The width at the end of the silicon nanowire is tapered from 450 nm to a tiny tip end of 40 nm so that the guided mode will expand into a polymer waveguide, surrounding the SOI waveguide and the taper. The device has a silicon-on-insulator (SOI) structure, with the silicon waveguide placed on a SiO_2/Si substrate. The measured propagation loss is 4.3 dB/cm and the fiber-to-fiber loss of the device is 6.8 dB.

The experimental setup for the silicon chip based 160 Gbit/s optical packet switching is shown in Fig. 1. It mainly includes a 160 Gbit/s RZ-OOK transmitter, an optical packet switch and a 160 Gbit/s OOK receiver. The erbium-glass oscillating pulse-generating laser (ERGO-PGL) produces 10 GHz pulses at 1542 nm with a 1.5-ps full-width at half-maximum (FWHM) pulse width. The 10-GHz pulses are launched into a 400-m dispersion-flattened highly non-linear fiber (DF-HNLF, dispersion D = -0.45 ps/nm/km and dispersion slope S = 0.006 ps/nm^2/km at 1550 nm, nonlinear coefficient γ = 10.5 W^{-1}km^{-1}) to generate a supercontinuum based on self-phase modulation (SPM) [9]. At the output of the DF-HNLF, the broadened spectrum is filtered with a 5 nm optical band pass filter (OBF) centered at 1562 nm to generate 10 GHz pulses for the data signal and is also filtered at 1538 nm using a 1 nm OBF to obtain the 10 GHz control pulses used in the 160 Gbit/s OOK receiver. The wavelength converted and compressed pulses are on-off keying (OOK) modulated using a software defined pattern to generate 10 Gbit/s Ethernet packets in a Mach-Zehnder modulator (MZM). The Ethernet packet with a maximum standardized size of 1518 bytes consists of a preamble, a destination address, a source address, an Ethertype, payload data and a frame check sequence (FCS). The packets have a duration of 2.19 µs, consisting of 1.22 µs of data payload separated by a 0.97 µs guard band. The generated 10 Gbit/s Ethernet packet is multiplexed in time to 160 Gbit/s using a passive fiber-delay multiplexer (MUX ×16).

In the optical packet switch, the generated 160 Gbit/s optical packet is amplified by an EDFA, then filtered by a 5 nm OBF and finally launched into the silicon nanowire through a 3-dB optical coupler (OC). The launched average data signal power is 13.5 dBm. The optical control signal is generated from a CW light at 1546 nm, which is modulated by an electrical control signal in a Mach-Zehnder modulator. The control signal has a duration of 1.5 µs and the launched average power is 8.5 dBm. The optical control signal is also launched into the silicon nanowire through the second input of the 3-dB coupler. Since the total launched power is well below the two

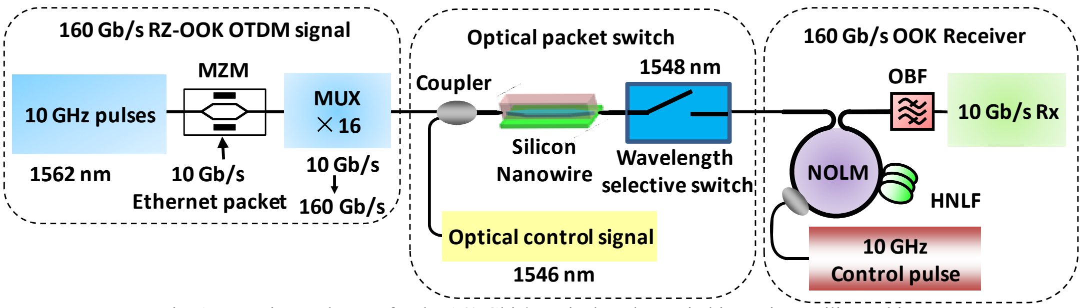

Fig. 1. Experimental setup for the 160 Gbit/s optical packet switching using a silicon chip.

photon absorption (TPA) threshold [3], the TPA and resulting carrier effects are negligible. The polarizations of the data signal and control signal are aligned to TE polarization into the silicon waveguide. At the output of the silicon nanowire, a wavelength selective switch (WSS) is used to switch the selected packet. The WSS is a red-shifted off-center filter compared to the control signal wavelength. The 160 Gbit/s optical packets modulate the refractive index of the silicon waveguide and generate cross-phase modulation (XPM) on the control signal. Only if there is a control signal, it will be phase modulated by the 160 Gbit/s optical packet and be converted into an amplitude modulated signal by passing through an off-center filter. Note that the refractive index of the silicon waveguide could also be modulated by an electrical signal [10], therefore, in principle the scheme could also work if the electrical signal is directly employed on the silicon chip.

The packet switched 160 Gbit/s RZ-OOK signal is detected by a 160 Gbit/s OOK receiver which consists of a nonlinear optical loop mirror (NOLM) based OTDM demutiplexer, a 0.9-nm filter, a photodetector (PD) and an error analyzer. The NOLM is used to OTDM demultiplex the 160 Gbit/s packet to a 10 Gbit/s packet based on cross-phase modulation (XPM) in a 50 m long HNLF. Finally, the demultiplexed 10-Gbit/s RZ-OOK signal is detected by the PD. An error analyzer is used to evaluate the performance of the packet switched signal.

III. Experimental results

Fig. 2 shows the oscilloscope traces of the optical packets before and after the packet switch. When 1 of 4 packets is aligned in time with the optical control signal, the packet is successfully switched with an extinction ratio of ~18 dB. The spectra at the input and the output of the silicon nanowire are shown in Fig. 3. Cross phase modulation on the CW light can be clearly seen at the output of the silicon nanowire. The blue part and the red part of the phase modulated spectrum are generated from the rising edge and falling edge of the 160 Gbit/s signal, respectively. A red-shift off-center filter at 1548 nm is used to obtain amplitude modulated 160 Gbit/s signal and separate the switched packet from the original packet.

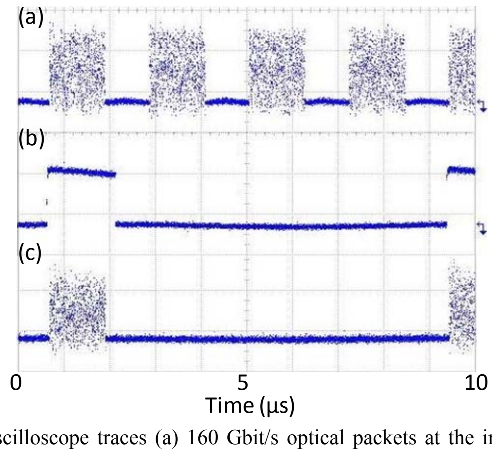

Fig. 2. Oscilloscope traces (a) 160 Gbit/s optical packets at the input of the silicon chip; (b) optical control signal; (c) 1 of 4 packet switched at the output of the silicon chip and wavelength selective switch.

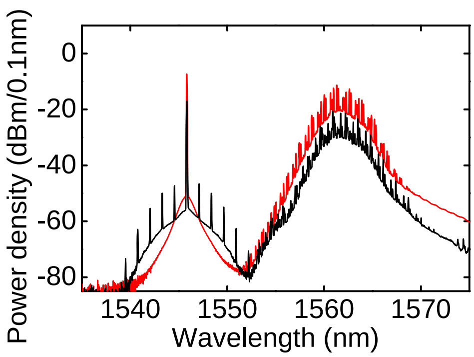

Fig. 3. Optical spectra at the input of the silicon chip (red) and output of the silicon nanowire (black).

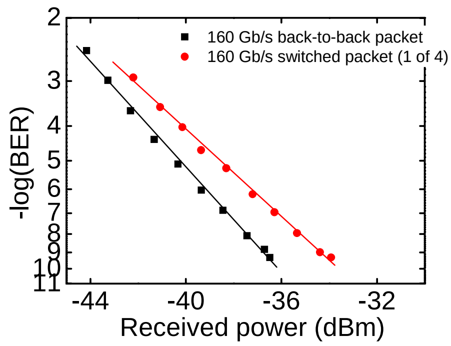

Fig. 4. BER measurements after demultiplexing to 10 Gbit/s for the 160 Gbit/s back-to-back packet and for the 160 Gbit/s 4-to-1 switched packet.

BER measurements after demultiplexing to 10 Gbit/s of the 160 Gbit/s switched packets are shown in Fig. 4 as a function of the received power. BER curves are plotted for the 160 Gbit/s back-to-back packets and for the 160 Gbit/s 4-to-1 switched packets. The 160 Gbit/s 4-to-1 switched packets achieve an error-free performance (BER 10^{-9}) with a power penalty of ~2.5 dB compared to the back-to-back case. The measured penalty is partly attributed to the pulse broadening due to the filtering, and partly attributed to the OSNR degradation after the packet switch due to the limited phase modulation on the control signal.

IV. Conclusion

We have successfully demonstrated 160 Gbit/s all-optical packet switching using a silicon chip. The 4-to-1 switched 160 Gbit/s packet shows error free performance, and holds great promise for potential future all-optical packet switches of ultra-fast data signals.

V. Acknowledgment

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